CLAIMS

1. An integrated circuit (IC) comprising:

a first transistor comprising a first floating gate and a first control gate;

a second transistor comprising a second floating gate and a second control gate, the second floating gate being electrically connected to the first floating gate; and

a third transistor comprising a third floating gate and a third control gate, the third floating gate being electrically connected to the third control gate.

2. The IC of Claim 1, wherein the first transistor and the third transistor are matched transistors.

3. The IC of Claim 2, wherein a physical gate area of the second transistor is substantially larger than a channel area of the second transistor.

4. The IC of Claim 1, wherein the second floating gate is formed on an oxide layer, and wherein a portion of the oxide layer is thinned to provide a programming window.

5. The IC of Claim 1, further comprising:

an input terminal; and

a comparator, wherein the first transistor is connected between the input terminal and a first input of the comparator, and wherein the second transistor is connected between the input terminal and a second input of the comparator.

6. The IC of Claim 5, wherein the third control gate is connected to the input terminal, and

wherein the first control gate is connected to the second control gate.

7. The IC of Claim 6, wherein the second transistor further comprises a source and a drain, the source and drain being formed in a substrate,

wherein the reference voltage circuit further comprises a programming control circuit configured to provide a first voltage to the source and the drain of the second transistor and provide a second voltage to the second control gate when a programming signal is asserted, wherein the first voltage and the second voltage are sized to cause charge transfer between the substrate and the floating gate, and

wherein the programming control circuit is further configured to provide the first voltage to the second control gate and provide the second voltage to the source and drain of the second transistor when a reset signal is asserted.

8. The IC of Claim 7, further comprising an output control circuit configured to assert a control signal in response to a comparator output signal from the comparator indicating that an output from the first transistor is greater than an output from the third transistor, wherein the programming control circuit removes the first voltage from the source and the drain of the second transistor when the control signal is asserted.

9. The IC of Claim 8, wherein the output control circuit is further configured to provide the comparator output signal as an indicator signal when neither the programming signal nor the reset signal is asserted.

10. A method for creating a reference voltage circuit, the method comprising:

forming a first transistor having a first floating gate and a first control gate;

forming a second transistor having a second floating gate and a second control gate;

electrically connecting the second floating gate to the first floating gate;

forming a third transistor having a third floating gate and a third control gate; and

electrically connecting the third floating gate to the third control gate.

11. The method of Claim 10, wherein forming the third transistor comprises matching the third transistor to the first transistor.

12. The method of Claim 11, wherein forming the second transistor comprises sizing the second floating gate larger than the first floating gate.

13. The method of Claim 10, wherein forming the second transistor comprises:

providing an oxide layer;

thinning a first portion of the oxide layer;

forming the second floating gate on the oxide layer.

14. The method of Claim 10, wherein the first floating gate, the second floating gate, and the third floating gate are formed during a first polysilicon process step, and

wherein the first control gate, the second control gate, and the third control gate are formed during a second polysilicon process step.

15. A voltage reference circuit comprising:

an input terminal;

a first transistor having a first floating gate;

a second transistor having a second floating gate and a second control gate, the second control gate being electrically connected to the input terminal and the second floating gate; and

a comparator, wherein the first transistor is connected between the input terminal and a first input of the comparator, and wherein the second transistor is connected between the input terminal and a second input of the comparator.

16. The voltage reference circuit of Claim 15, wherein the first transistor and the second transistor are matched transistors.

17. The voltage reference circuit of Claim 15, further comprising a third transistor having a third floating gate, the third floating gate being electrically connected to the first floating gate.

18. The voltage reference circuit of Claim 17, wherein a physical gate area of the third transistor is substantially larger than a channel area of the third transistor.

19. The voltage reference circuit of Claim 17, further comprising a programming control configured to program the first

transistor by applying a programming voltage to a source and a drain of the third transistor and applying a first offset voltage to a control gate of the third transistor, wherein the source and the drain of the third transistor are formed in a substrate, and wherein the programming voltage and the first offset voltage are sized to cause charge transfer between the substrate and the third floating gate.

20. The voltage reference circuit of Claim 19, wherein the programming control circuit is further configured to erase the first transistor by applying an erase voltage to a control gate of the third transistor and applying a second offset voltage to the source and the drain of the third transistor, the erase voltage and the second offset voltage being sized to cause charge transfer between the third floating gate and the substrate.

21. The voltage reference circuit of Claim 15, wherein the first floating gate has a net charge that causes the first transistor to provide a first voltage to the first input terminal of the comparator when a second voltage is applied to a control gate of the first transistor, and

wherein the second transistor provides the first voltage to the second input terminal of the comparator when a reference voltage is applied to the input terminal.

22. A method for comparing a test voltage to a reference voltage, the method comprising:

providing a charge on a floating gate of a first transistor, the charge being sized such that applying a first voltage to a control gate of the first transistor results in a source voltage of the first transistor being

equal to a source voltage of a second transistor when the reference voltage is applied to a floating gate of the second transistor;

applying the first voltage to the control gate of the first transistor;

supplying the test voltage to the floating gate of a second transistor;

supplying the test voltage to a drain of the first transistor and to a drain of the second transistor; and

comparing the source voltage of the first transistor to the source voltage of the second transistor.

23. The method of Claim 22, wherein the first transistor and the second transistor are matched transistors.

24. The method of Claim 22, wherein the first voltage is a ground voltage.

25. A method for programming a reference voltage into a storage transistor, the method comprising:

providing a programming potential across a first transistor to generate a net charge on a floating gate of the first transistor;

providing a second transistor, wherein a floating gate of the second transistor is connected to the floating gate of the first transistor;

supplying the reference voltage to a control gate of a third transistor, wherein the control gate of the third transistor is electrically connected to a floating gate of the third transistor;

supplying the reference voltage to a drain of the second transistor and to a drain of the third transistor; and

removing the programming potential across the first transistor when an output of the second transistor becomes equal to an output of the third transistor.

26. The method of Claim 25, wherein the second transistor and the third transistor are matched transistors.

27. A method for comparing a test voltage to a reference voltage, the method comprising:

providing a first transistor, wherein a first terminal coupled to a test voltage input terminal, a second terminal, a floating gate, and a control gate, wherein the floating gate of the second transistor is electrically connected to the control gate of the second transistor;

providing a charge on the floating gate of the first transistor, the charge being sized such that when a first voltage is applied to the control gate of the first transistor, an output at the second terminal of the first transistor is equal to an output at the second terminal of the second transistor when the reference voltage is applied to the floating gate of the second transistor;

applying the first voltage to the control gate of the first transistor;

supplying the test voltage via the test voltage input terminal; and

comparing the output at the second terminal of the first transistor to the output at the second terminal of the second transistor.

28. The method of Claim 27, wherein the first transistor and the second transistor are matched transistors.

29. The method of Claim 27, wherein the first voltage is a ground voltage.

30. The method of Claim 27, further comprising:

placing an output signal in a first state when the differential output indicates that an output from the first transistor is greater than an output from a second transistor, wherein the first state indicates that the reference voltage is greater than the test voltage; and

placing the output signal in a second state when the differential output indicates that the output from the first transistor is less than the output from the second transistor, wherein the second state indicates that the reference voltage is less than the test voltage.

31. A floating gate transistor comprising:

a source;

a drain;

a channel region between the source and the drain;

a floating gate over the channel region;

a control gate over the floating gate, wherein the control gate is electrically connected to the floating gate;

a first dielectric layer between the channel region and the floating gate; and

a second dielectric layer between the floating gate and the control gate.

32. The floating gate transistor of Claim 31, wherein the control gate is electrically connected to the drain.

33. A floating gate transistor, wherein a physical gate area of the floating gate transistor is substantially greater than a channel area of the floating gate transistor.

34. The floating gate transistor of Claim 33, comprising:

a source region;

a drain region;

a channel region between the source region and the drain region;

a floating gate over the channel region; and

a control gate over the floating gate, wherein the control gate and the floating gate both extend beyond the source region.